PCI 9080RDK-860 Hardware Reference Manual

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1. Introduction

1.1 About This Manual

This manual provides information about the design of the 9080RDK-860 evaluation board. It contains a description of all the major functional areas on the board, with explanations where required. It also appends a bill of materials, and a complete schematic.

The 9080RDK-860 evaluation board has been tested with the PCI SDK Release 1.2.

Please contact PLX's Customer Support for information on purchasing other PLX Reference Design Kits.

1.2 Where To Go From Here

The following is a brief summary of the chapters to help guide your reading of this manual:

Chapter 2, General Information, is an overview of the PCI 9080RDK-860 as well as conventions and terminology used throughout this manual.

Chapter 3, RDK Hardware Installation, provides instructions for installing the evaluation board.

Chapter 4, Hardware Design, provides details of the evaluation board design.

Chapter 5, Customer Support, provides information on how to contact PLX Customer Support.

Chapter 6, Schematics, provides hardware schematics for the evaluation board.

Chapter 7, Bill of Materials, provides a bill of materials for the evaluation board.

2. General Information

2.1 Introduction

The 9080RDK-860 evaluation board enables designers to learn the features and design issues of the PCI 9080 by using the chip in a board before designing it into their own designs. When used with the PCI SDK software product, designers can test and evaluate the PCI 9080 device using the provided sample software, as well as implementing and testing user modified software that is aimed at a specific application. We are confident that through the use of this RDK, your designs will be brought to market faster and more efficiently.

2.2 Features

The PCI 9080RDK-860 evaluation board includes the following features:

- A Motorola MPC 860 microprocessor running at 40MHz;
- 16MB DRAM memory, upgradable to 32MB using standard 72-pin SIMMs;
- 512KB SRAM memory;
- 512KB FLASH memory;
- One serial communications port using the MPC860 on-board UART (RS-232 compatible);
- Reset switch;
- Debug LEDs;
- Headers are provided for debug and expansion;
- Prototype area;

2.3 Terminology

All signals and device pin names are *italized.*

Signals are either active high or active low. Active low signals are defined as true (asserted) when they are at a logic low. Similarly, active high signals are defined as true when they are at a logic high.

3. RDK Hardware Installation

3.1 PCI 9080RDK-860 Hardware Installation

To install the PCI 9080RDK-860 evaluation board, please follow these steps to prevent electrostatic damage to the host computer and to the evaluation board.

- Log off and shut down the host computer;
- Turn off the power to the system and disconnect the power cord. Make sure the chassis and the unopened anti-static shipping bag in which the PCI 9080RDK-860 evaluation board was packed are properly grounded, preferably at an anti-static workstation with wrist-straps;
- Remove the case from the computer and remove the PCI 9080RDK-860 evaluation board from the anti-static packaging;
- Place the PCI 9080RDK-860 evaluation board in an empty PCI slot. Picking a slot which is accessible to test equipment may be a requirement; and

Note: *It may be preferable to use a PCI slot extender to have more space with which to work.*

- Replace the captive screw to ensure proper electrical grounding and mechanical stability.

This completes the hardware installation.

3.2 Verifying Installation

To verify that the hardware has been installed properly, install the PCI SDK (please refer to PCI SDK User's Manual) and double click on the *PLXMon97* icon located in the PCI SDK folder. If the *PLXMon97* application starts properly it should select the 9080RDK-860 device by default. If the verification was not successful uninstall all software, verify that the hardware is installed properly, and reinstall all the software. If this is not successful please contact Customer Support (see chapter 5 for information on contacting Customer Support).

4. Hardware Design

This section contains a detailed description of each sub-section on the evaluation board. It also contains a trouble shooting section to aid designers in solving typical problems.

4.1 Hardware Description

Figure 4-1 shows the location of important devices and connectors on the evaluation board.

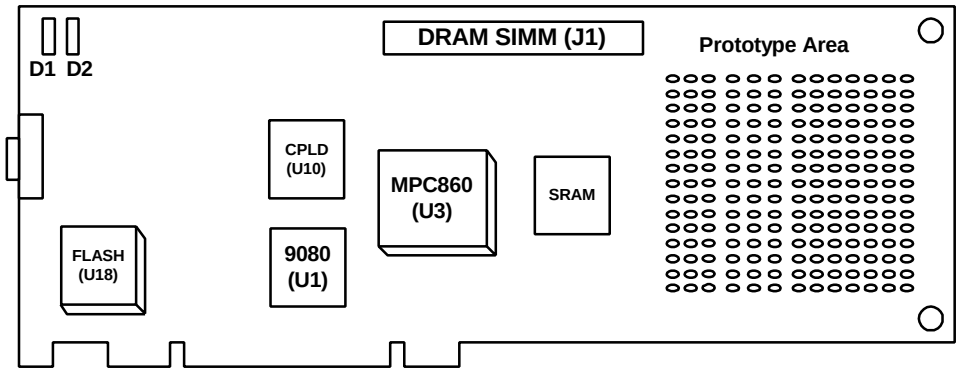


Figure 4-1 PCI 9080RDK-860

4.1.1 9080RDK-860 Memory Map

The memory map in Figure 4-2 shows the location of all devices which may be accessed through the 9080 device and the MPC860 processor. All external memory devices are accessed using the MPC860 on-board memory controller.

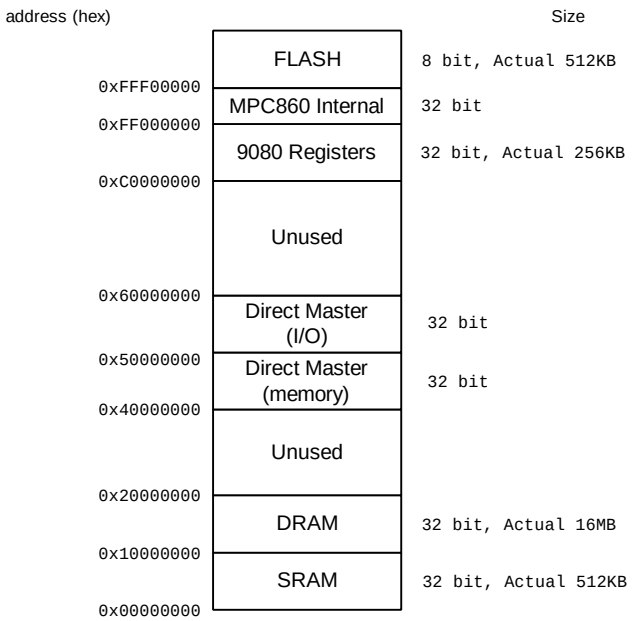


Figure 4-2 Memory Map

External Memory Device	MPC860 Memory Control
FLASH	CS0~, GBCS
DRAM	CS1~, UPMA
SRAM	CS2~, GPCM2
PCI9080 Registers	CS3~, GPCM3

4.1.2 9080RDK-860 Interrupts

The evaluation board has two external interrupt sources that are connected as shown in the table below.

Interrupt Line	Usage
IRQ1	PCI9080 (*LINTO~*)
IRQ7	PCI9080 Error (*LSERR~*)

4.1.3 FLASH Socket

U18 is a socket that contains a FLASH memory device. The FLASH shipped with the kit is a 512K x 8, 90 ns FLASH, containing PLXRom-860. At reset the MPC860 executes the program stored in the FLASH at offset 0x0060000. The RDK also supports on-board FLASH programming through use of PLXLdr.

4.1.4 PCI 9080 Configuration Socket

U2 is a socket that contains a serial EEPROM. The serial EEPROM shipped with the kit is a 128 x 8, 3-wire bus serial EEPROM. This EEPROM holds the PCI 9080 configuration data. The 9080 has been configured using the *SHORT~* pin to do a long configuration. The contents of the configuration EEPROM can be displayed using PlxMon97's *'re'* command.

4.1.5 DRAM SIMM Socket

J1 is a connector that contains a 72-pin, 16MB, 60 ns DRAM SIMM. The DRAM is controlled using the MPC860 memory controller. If other DRAM speeds are used, designers may be required to modify the DRAM controller logic.

The DRAM controller has been written to use 60 ns, fast page-mode SIMMs and is upgradable to 32MB.

4.1.6 LEDs

The evaluation board contains two LEDs to inform the user of certain conditions and events. The function of each LED is listed below.

LED	Purpose
D1 (Green)	Debug LED. This LED is directly connected to the *USERO~* pin of the 9080.
D2 (Red)	FRZ LED. This LED is connected directly to the FRZ~ pin of the MPC860.

4.1.7 Lattice Configuration Header

JP8 is a header that is used to program the Lattice CPLD device. The CPLD is pre-configured during manufacturing and should only be used by users who wish to change the CPLD logic. The header conforms to the standard pin-out used by Lattice ISP development tools.

4.1.8 Local Bus Reset

The local bus can be reset by four different methods (Figure 4-3): At power-up, low voltage, manually using switch SW1, or the PCI 9080 *LRESETO~* signal.

U21 is a power supervisor device that handles the first three local bus reset methods. A local bus reset causes the following devices to enter reset state: The MPC860, Lattice CPLD, and the UART. **Note: The PCI 9080 is not reset by U21.**

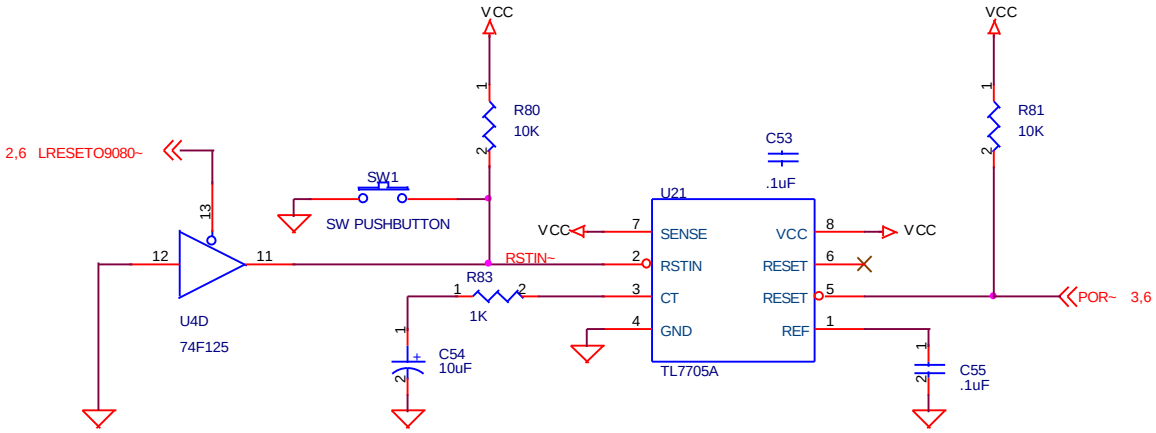


Figure 4-3 Reset Circuitry

4.1.9 RS-232 Connector

P1 is a 9 pin DB-9 Male RS-232 connector. A null modem cable is required when connecting to a serial port of a computer. An appropriate cable is provided with the RDK.

4.1.10 Prototype Area

The right side of the evaluation board contains a prototype area.

All the holes in the center grid are plated, but not connected to anything. For prototyping, extra components may be placed, and soldered, in this area, and connected together or to other parts on the board.

4.1.11 Power Supply Design

The evaluation board has two power planes: VCC and GND. The VCC plane powers all local bus devices and has a 3.3 volt 'island' within it for the MPC860. The 3.3 volts is drawn from U19, a 3A regulator, by default. JP11 can be installed if it is desired to draw power directly from the PCI bus. However, most PCI buses do not supply 3.3v and therefore this method is not recommended.

The PCI 9080 device draws power from two different sources. The 9080's PCI bus interface is

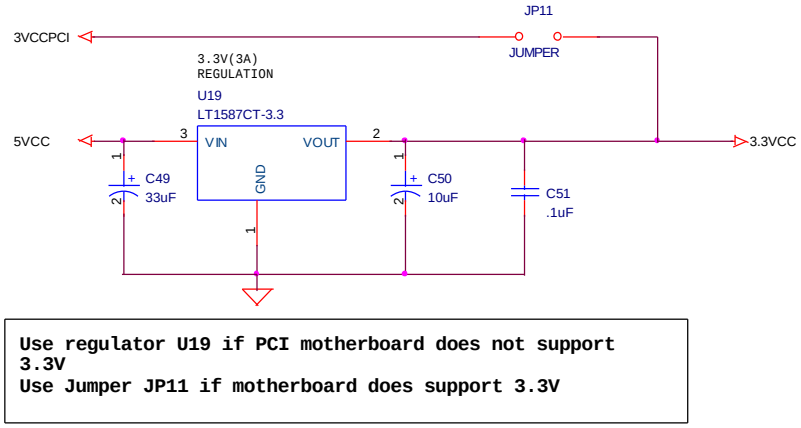


Figure 4-4 Local Bus Power Supply

switchable between 5 volts and 3.3 volts internally and is powered by the PCI bus *+VI/O* pins. The local bus interface is fixed at 5 volts and draws power from the PCI bus *+5VCC* pins.

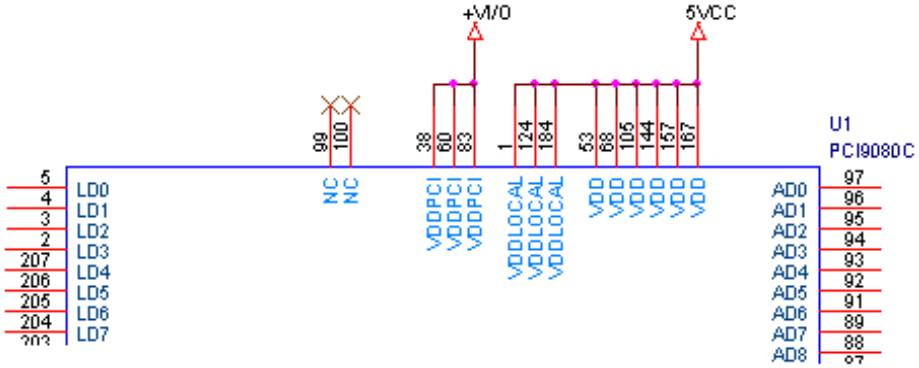


Figure 4-5 PCI 9080 Power Supply

4.1.12 PCI 9080 Design Highlights

The following points are provided to highlight certain design characteristics of the evaluation board:

- *SHORT*~ is configured for a long Serial EEPROM load;
- Direct Master is configured to use the 9080 internal memory decoder;
- PCI 9080 is configured in CA bus mode;
- *NB*~ is pulled-up. Therefore, the FLASH software must set the PCI 9080 local init bit.

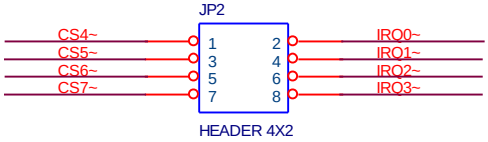
4.1.13 Evaluation Board Headers and Connectors

Below is a description of all headers and connectors on the evaluation board.

Item	Description
JP1	JTAG Port. This header conforms to the JTAG standard and can be used during testing and debugging.

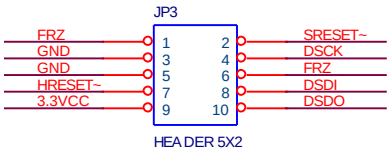
Item	Description
JP2	Interrupt/ Chip Select. This header provides access to unused MPC860 chip selects and interrupt request lines.

Interrupt/ Chip Select



Item	Description
JP3	Debug Development Port. This header conforms to the MPC860 Debug Development Port standard and should be used by MPC860 emulation tools.

Development Port



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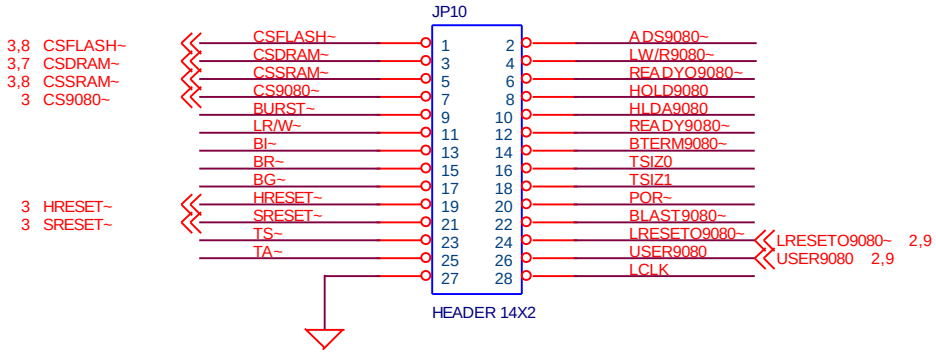
Item	Description
P1	RS-232 Connector. Please consult Section 4.1.9 for more information.

Item	Description
JP4, JP5, JP6, JP7	MPC860 Expansion Headers. These headers provide access to unused MPC860 I/O pins. Please consult the 860RDK schematic for a pin-out diagram.

Item	Description
JP10	Local Bus Header. This headers provides access to commonly used local bus signals.



Item	Description
J2	Universal PCI Edge Connector (Figure 4-6). The PCI Edge connector supports either a 3.3 volt PCI bus or a 5 volt PCI bus.

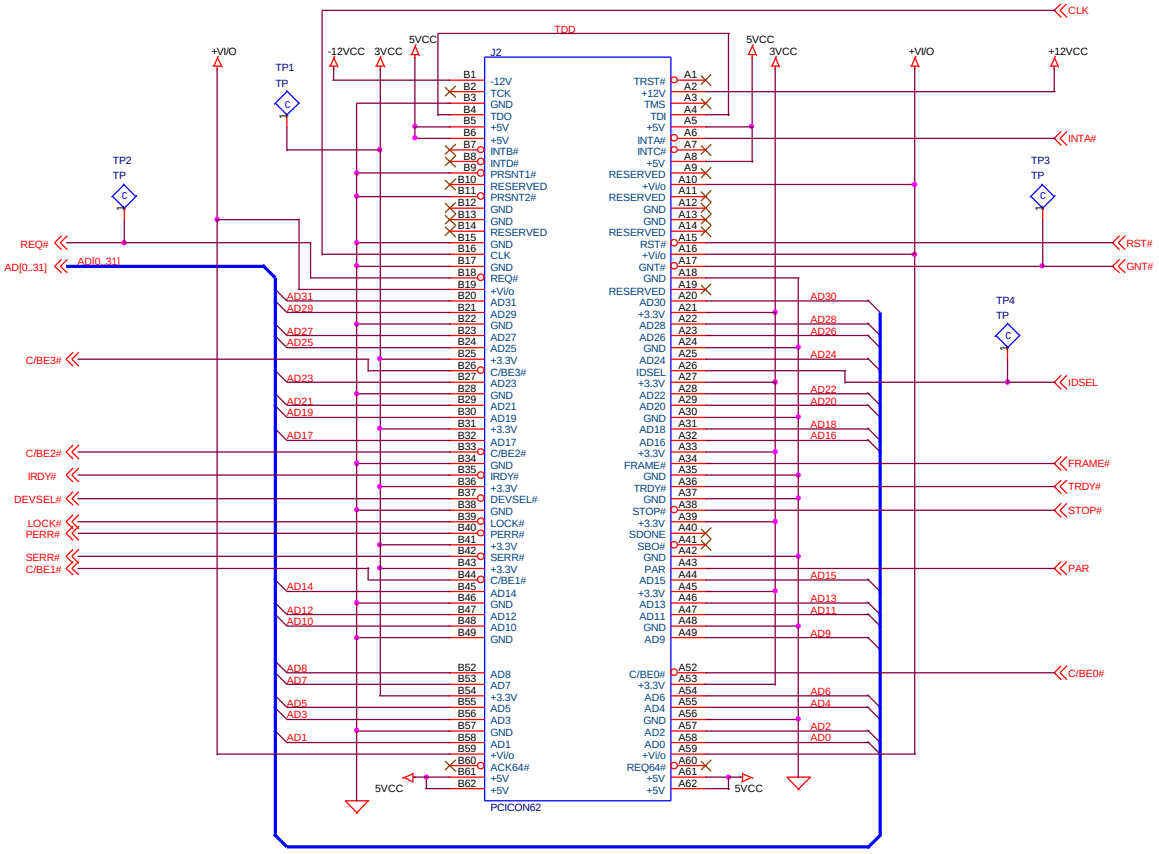


Figure 4-6 PCI Edge Connector

Item	Description
J2	Local Data Bus (Figure 4-7). This header contains the full 32-bit data bus.

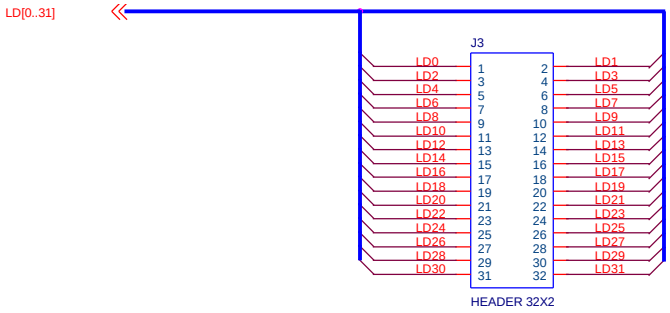


Figure 4-7 Local Data Bus

Item	Description
J3	Local Address Bus (Figure 4-8). This header contains the full 32-bit Address bus.

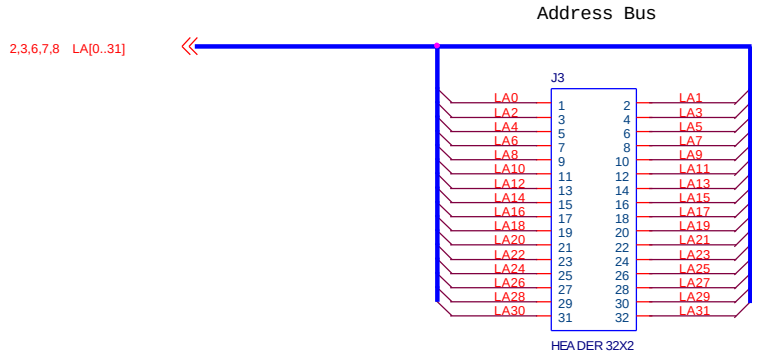


Figure 4-8 Local Address Bus

4.1.14 Lattice CPLD Design

Users should consult the appropriate PLX Technology Application note for CPLD design information.

4.2 Troubleshooting

If the board is not functioning properly the following table may help in determining the problem:

Problem	Corrective Action
D1 and D2 stay lit	Lattice CPLD has not been programmed.
D2 stays lit after reset	MPC860 has entered the Debug Mode. Be sure nothing is connected to the development port
D2 lights during program execution	A system error has occurred.
Cannot download user software	The Vendor ID and Device ID must be 0x10b5, 0x0860.
Cannot boot computer	The FLASH image is not correct. The boot software must set the local init bit of the PCI 9080 before a boot can continue.

5. Customer Support

Prior to contacting customer support, please ensure you have the following information:

1. You are situated close to the computer that has the RDK installed;
2. Serial Number of the evaluation board;
3. Type of processor on the evaluation board;
4. Operating System version and type; and
5. Description of problem.

You may contact PLX customer support at:

Address: PLX Technology, Inc.
390 Potrero Avenue
Sunnyvale, CA 94086

Phone: 408-774-9060
Fax: 408-774-2169
Web: http://www.plxtech.com

6. Schematics

The following pages are re-printed hardware schematics of the evaluation board.

7. Bill of Materials

The following pages are re-printed bill of materials of the evaluation board.

This reference design kit has been developed and tested by Vitana Corporation.
For more information regarding SDK and RDK designs, please contact:

Vitana Corporation
Tel: 613-749-4445
Email: rdk@vitana.com
Web: www.vitana.com

For technical support questions, please contact PLX Customer Support